Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONSl**

1. **OUTPUT**
2. **ADJ**
3. **OUTPUT**
4. **INPUT**
5. **OUTPUT**

**.071”**

**.110”**

**1**

**2**

**5**

**4**

**3**

**MASK**

**REF**

**LM1086A ADJ**

**Top Material: Al**

**Backside Material: Ti/Ni/Ag**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND Backside Potential is VOUT**

**Mask Ref: LM1086A**

**APPROVED BY: DK DIE SIZE .071” X .110” DATE: 3/15/23**

**MFG: NATIONAL THICKNESS .013” P/N: LM1086-ADJ-MDC**

**DG 10.1.2**

#### Rev B, 7/1